

A tool for advanced learning of LFSR-based testing principles

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 175-178 : ill

A tool for teaching pseudo-random TPG principles

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes Proceedings of the 17th EAAEIE Annual Conference on Innovation in Education for Electrical and Information Engineering : Craiova, Romania, June 1st-3rd, 2006 2006 / p. 182-187 : ill

Automated software-based in-field self-test program synthesis

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton International journal of microelectronics and computer science 2017 / p. 57-64 : ill

Automated software-based self-test generation for microprocessors

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton Proceedings of the 24st International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2017 : Bydgoszcz, Poland, June 19-21, 2014 2017 / p. 453-458 : ill
<https://doi.org/10.23919/MIXDES.2017.8005252>

Automatic SoC level test path synthesis based on partial functional models

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 <https://ieeexplore.ieee.org/document/6114730>

Automation of testing beyond the SoCs

Tšertov, Anton; Jutman, Artur; Devadze, Sergei Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 29-32 : ill

BIST analyzer : a training platform for SoC testing [Electronic resource]

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 37th Annual Frontiers in Education Conference : Global Engineering : Knowledge Without Borders, Opportunities Without Passports : Milwaukee, Wisconsin, October 10-13, 2007 2007 / p. S3H-8-S3H-13 : ill. [CD-ROM] <http://dx.doi.org/10.1109/FIE.2007.4418125>

Calculation of LFSR seed and polynomial pair for BIST applications

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 105-108 : ill

Calculation of LFSR seed and polynomial pair for BIST applications [Electronic resource]

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 275-279 : ill. [CD-ROM]

E-learning environment for WEB-based study of testing

Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan; Devadze, Sergei; Jenihhin, Maksim; Aleksejev, Igor; Tšepurov, Anton; Tšertov, Anton; Kostin, Sergei; Orasson, Elmet; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 2010 / p. 47-52 : ill

Hardware/Software co-design in practice : MEMOCODE'08 contest experience

Reinsalu, Uljana; Devadze, Sergei; Jutman, Artur; Tšertov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 55-58 : ill

High-level modeling and testing of multiple control faults in digital systems

Jasnetski, Artjom; Oyeniran, Adeboye Stephen; Tšertov, Anton; Schölzel, Mario; Ubar, Raimund-Johannes Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill <http://dx.doi.org/10.1109/DDECS.2016.7482445>

High-level test data generation for software based self-test in microprocessors

Oyeniran, Adeboye Stephen; Jasnetski, Artjom; Tšertov, Anton; Ubar, Raimund-Johannes 2017 6th Mediterranean Conference on Embedded Computing (MECO) : including ECYPS'2017 : proceedings : research monograph : Bar, Montenegro, June 11th-15th, 2017 2017 / p. 86-91 : ill <https://doi.org/10.1109/MECO.2017.7977167>

IEEE 1687 compliant ecosystem for embedded instrumentation access and in-field health monitoring

Tšertov, Anton; Jutman, Artur; Shibin, Konstantin; Devadze, Sergei IEEE AUTOTESTCON 2018 : National Harbor, September 17-20, 2018 : proceedings 2018 / 9 p.: ill <https://doi.org/10.1109/AUTEST.2018.8532559>

In-system programming of non-volatile memories on microprocessor-centric boards

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2014 / p. 25-34 : ill

Laboratory framework TEAM for investigating the dependability issues of microprocessor systems

Jasnetski, Artjom; Tšertov, Anton; Ubar, Raimund-Johannes; Kruus, Helena 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 80-83 : ill

Microprocessor modeling for board level test access automation

Devadze, Sergei; Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes Proceedings of 10th IEEE Workshop on RTL and High Level Testing : Hong Kong, November 27-28, 2009 2009 / ? p

Microprocessor-based system test using debug interface

Devadze, Sergei; Jutman, Artur; Tšertov, Anton; Instenberg, Martin; Ubar, Raimund-Johannes 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 98-101 : ill <http://dx.doi.org/10.1109/NORCHIP.2008.4738291>

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; Raik, Jaan; Tšertov, Anton; Ubar, Raimund-Johannes 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

On automatic software-based self-test program generation based on high-Level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguaçu, Brazil, 6th-9th April 2016 2016 / p. 177 <http://dx.doi.org/10.1109/LATW.2016.7483357>

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2013 / p. 72-78 : ill

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2013, Gdynia, Poland, June 20-22, 2013 2013 / p. 408-413 : ill

Post-silicon validation of IEEE 1687 reconfigurable scan networks

Damljanovic, Aleksa; Jutman, Artur; Squillero, Giovanni; Tšertov, Anton 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791546>

Simulation-based equivalence checking between IEEE 1687 ICL and RTL

Damljanovic, Aleksa; Jutman, Artur; Portolan, Michele; Tšertov, Anton 2019 IEEE International Test Conference (ITC) 2019 / paper. 7.3, 8 p. : ill <https://doi.org/10.1109/ITC44170.2019.9000181>

SoC and board modeling for processor-centric board testing

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 14th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2011 : 31 August - 2 September 2011, Oulu, Finland : proceedings 2011 / p. 575-582 : ill

Software-based self-test generation for microprocessors with high-level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton; Brik, Marina Proceedings of the Estonian Academy of Sciences 2014 / p. 48-61 : ill https://artiklid.elnet.ee/record=b2665215*est

Software-based self-test generation for microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Tšertov, Anton; Jasnetski, Artjom; Brik, Marina LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Software-based self-test with decision diagrams for microprocessors

Ubar, Raimund-Johannes; Jasnetski, Artjom; Tšertov, Anton; Oyeniran, Adeboye Stephen 2018

A suite of IEEE 1687 benchmark networks

Tšertov, Anton; Jutman, Artur; Devadze, Sergei 2016 IEEE International Test Conference (ITC) : proceedings 2016 / art. 6.1, p. 1-10 : ill <https://doi.org/10.1109/TEST.2016.7805840>

System modeling for processor-centric test automation = Süsteemide modelleerimine protsessorikesksete testprogramme süntheesi automatiseerimiseks

Tšertov, Anton 2012 https://www.ester.ee/record=b2751131*est

Teaching digital test with BIST analyzer

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 19th EAAEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 123-128 : ill <http://dx.doi.org/10.1109/EAAEIE.2008.4610171>

Testing beyond the SoCs in a lego style

Tšertov, Anton; Jutman, Artur; Devadze, Sergei Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 334-338 : ill

Triple-triple redundant 777 primary flight computer

Tšertov, Anton A & A 2007 / 5, p. 38-47 : ill https://artiklid.elnet.ee/record=b1021108*est